# EB555 Schematic Directory

| SHEET | DESCRIPTION |
|---|---|
| sht 1 | Schematic Directory |
| sht 2 | Block diagram |
| sht 3 | 21555 (DrawBridge - 66MHz) |
| sht 4 | 21555 Parallel & Serial ROM, latches and MDM |
| sht 5 | Secondary clock generation & hot swap test |
| sht 6 | Pull up resistors for 21555 signals |
| sht 7 | Primary Edge Connector and svio generation |
| sht 8 | System Slot - PICMG or PCI Option |
| sht 9 | PCI Secondary Option slots Middle and Bottom |
| sht 10 | 3.3V Voltage regulator and bulk decoupling |
| sht 11 | Mictor Connectors |

1-7-2000_16:53

CDATE=1-NOV-1997

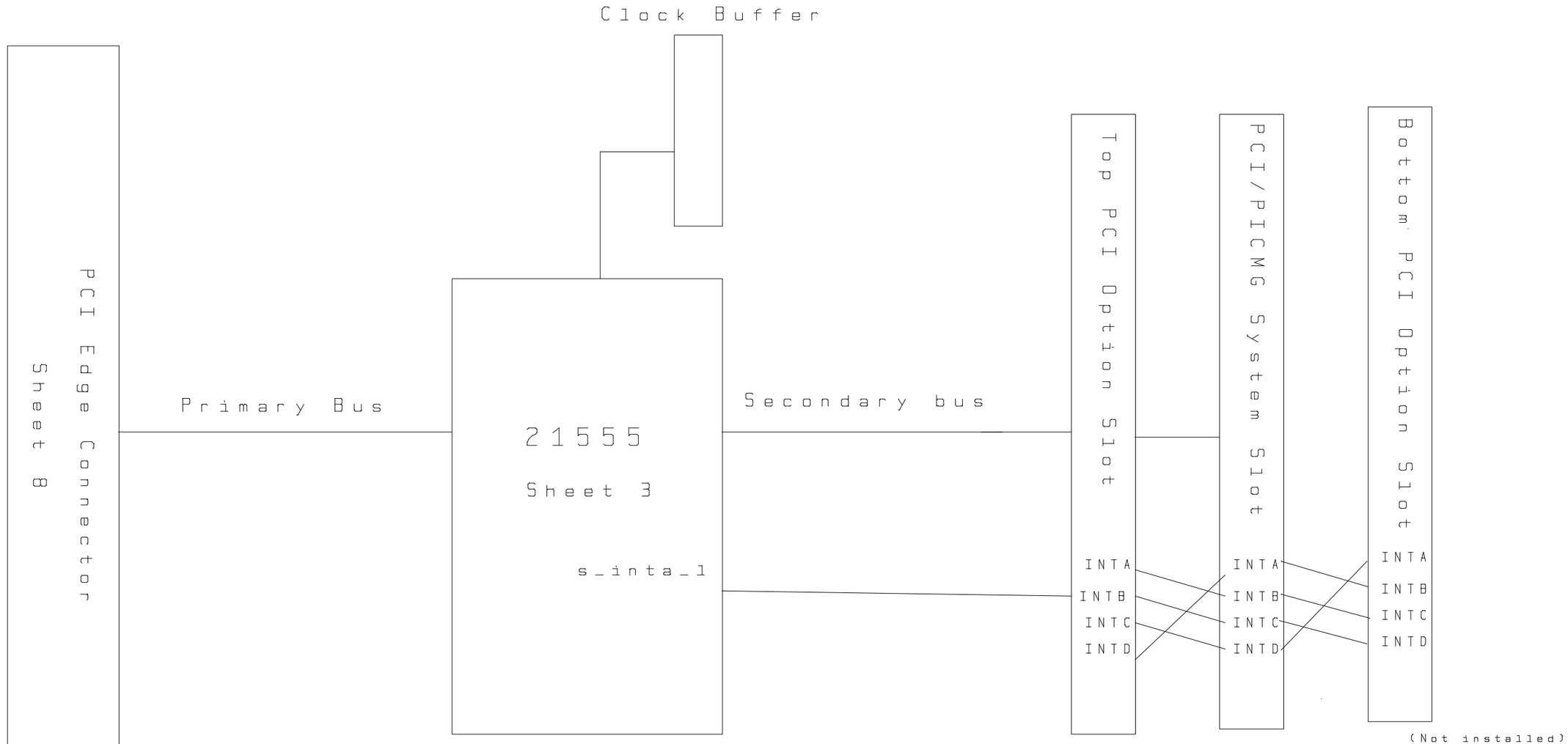
| REVISION | | |
|---|---|---|
| CHK | CHANGE NO. | REV |

EB555 21555 EVALUATION BOARD

intel

| | | | | | |
|---|---|---|---|---|---|
| DRN. | DATE | ENG. SMC | DATE | TITLE: EB555 | |
| CHK'D. | DATE | BOARD LOCATION: | | | |
| | | SHEET | OF | | |
| USRA: | | TOP DOCUMENT NUMBER: | | SIZE B | CODE / NUMBER / REV. |
| FIRST USED ON OPTION/MODEL: | | | | | |

# EB555 Block Diagram




1-12-2000_14:16

| | | | |
|---|---|---|---|
| ENG. SMC | DATE | TITLE: EB555 | 2 |
| BOARD LOCATION: | | | |
| SHEET | OF | | |
| TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER / REV. | |

E2

PCI-TO-PCI
64-64
DRAWBRIDGE

P_CLK R4
P_RST P1
P_GNT R1
P_IDSEL W1
PVIO U21
P_M66ENA AC9

P_REQ T3
P_PAR AA6
P_SERR AB5
P_PERR AC5
P_INTA P2
P_STOP AB4
P_DEVSEL AC4
P_TRDY AB3
P_IRDY Y5
P_FRAME AC3
P_REQ64 Y13
P_ACK64 AC13
P_PAR64 U20

P_PME T23
P_ENUM T22

R48 4.99K

P_CBE
0 AA9 AC6 Y4 W2 AA15 AC14 AB14 AA14 7

P_AD
0 AB13 AB12 AC12 AC11 Y11 AA10 AB10 AC10 AB9 Y9 AA8 AC8 AA7 Y7 AC7 AB6 AB1 AA3 AA1 Y3 W4 Y1 Y2 W3 V3 V1 V2 U1 U4 U2 T1 T2 U23 V22 V23 V21 W22 W23 W21 Y22 W20 Y21 AA22 Y20 AC23 AC22 AA21 AC21 AB21 Y19 AC20 AB20 AC19 AB19 AA18 AB18 AC17 Y17 AA17 AC16 AB16 AC15 Y15 AB15 63

Pinout = 21555 Date: 6/99

E2

PCI-TO-PCI
64-64
DRAWBRIDGE

S_CLKI G3
S_AD28 B7
SVIO T21
S_M66ENA A16
S_PME R23

S_CLKO G4
S_RST H1

R65 0

SCLK_D

DB_RST

S_CLKI
S_IDSEL
SVIO
S_M66ENA
S_PME

S_PAR A13
S_SERR B13
S_PERR C13
S_INTA H2
S_STOP C12
S_DEVSEL A12
S_TRDY B12
S_IRDY C11
S_FRAME A11
S_REQ64 A21
S_ACK64 C20
S_PAR64 C22

PVIO

R48 4.99K

E1 S_RST_IN

PICMG_RST

S_AD
0 D19 A20 C19 A19 B19 C18 A18 B18 D17 B17 A15 D15 B15 A14 B14 C14 A10 C9 B9 D9 A9 C8 A8 C7 B6 A6 B5 A5 C5 A4 D5 C4 A22 A21 P22 P21 N20 N23 N22 N21 M22 L22 L21 L23 L20 K21 K23 J21 J22 J23 H21 H22 H23 G21 G22 G23 F22 F23 E22 E23 E21 D22 D23 E20 63

Pinout = 21555 Date: 6/99

E2
21555

PCI-TO-PCI
64-64
DRAWBRIDGE
DC1093

S_GNT
0 E4 D1 D2 E3 E2 F3 F1 F2 G1 8
S_GNT0 DB_GNT1 S_GNT2 S_GNT3 S_GNT4 S_GNT5 S_GNT6 S_GNT7 S_GNT8

S_REQ
S_REQ0 B3
DB_REQ1 A3
S_REQ2 C3
S_REQ3 A2
S_REQ4 A1
S_REQ5 D4
S_REQ6 C1
S_REQ7 C2
S_REQ8 D3
0 8

S_CBE
0 A17 D13 D11 A7 C23 C21 A23 D20 7
S_CBE0 S_CBE1 S_CBE2 S_CBE3 S_CBE4 S_CBE5 S_CBE6 S_CBE7

TDI H3
TMS J4
TCK J2
TRST J3

TDO J1 TDO

TRST

R90 4.99K

R62 0

P3

SCAN_ENA

L_STAT R20 L_STAT

SR_CS K1 DB_SRCS
PR_CS/PR_RDY N3 PR_CS
PR_CLK N4 PR_CLK
PR_ALE N2 PR_ALE
PR_RD M2 PR_RD
PR_WR N1 PR_WR

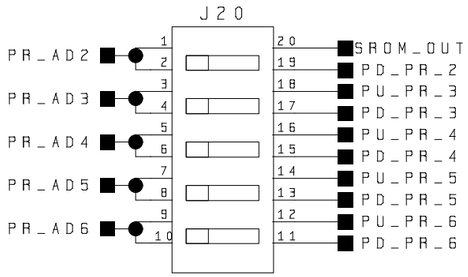
PR_AD
0 M1 M3 L3 L2 L1 L4 K3 K2 7
PR_AD0 PR_AD1 PR_AD2 PR_AD3 PR_AD4 PR_AD5 PR_AD6 PR_AD7

Pinout = 21554 (DC1093). Rev 0.4 Date: 7/1/97

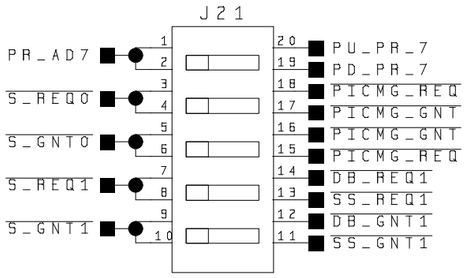
1-20-2000_6:04

| | | | |
|---|---|---|---|
| ENG. SMC | DATE | TITLE: EB555 3 | |
| BOARD LOCATION: | | | |
| SHEET OF | | | |
| TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER / REV. | |

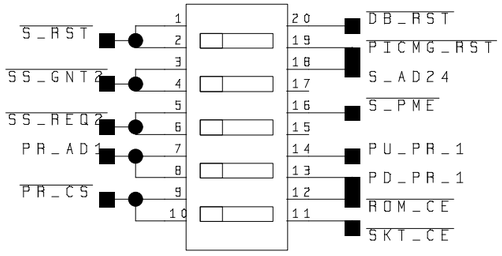
## Initialization Selections




| J20 | *DOWN = Pull DOWN* | *UP = Pull UP* |
|---|---|---|
| SW1 = pr_2 | NO SROM | SROM |
| SW2 = pr_3 | DEBUG – No Lockout | NORMAL – Lockout |
| SW3 = pr_4 | Synch | Async |
| SW4 = pr_5 | DB S_CLKO DISABLED | DB S_CLKO ENABLED |
| SW5 = pr_6 | 21554 as Central Function | System Slot as Central Function |

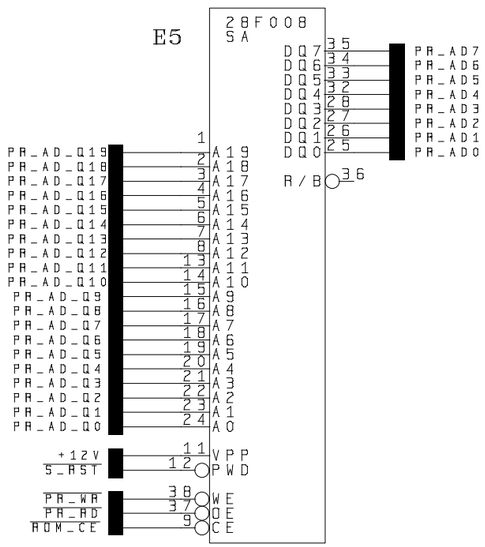



| J21 . . . | SYSTEM SLOT AS ARBITER | DRAWBRIDGE AS ARBITER |
|---|---|---|
| SW1=pr_ad7 | *DOWN* | *UP* |
| SW2=DB(s_req0) | *DOWN* | *UP* |
| SW3=DB(s_gnt0) | *DOWN* | *UP* |
| SW4=s_req1 | *DOWN* | *UP* |
| SW5=s_gnt1 | *DOWN* | *UP* |

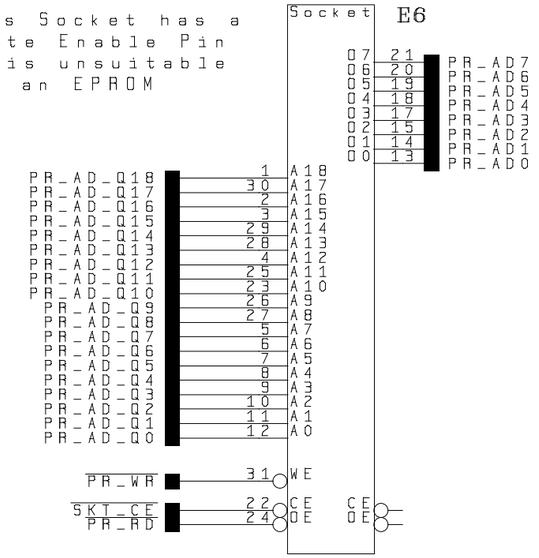


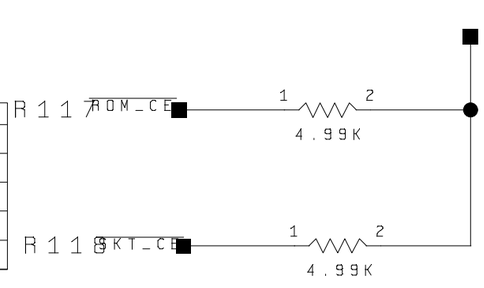

| J9 | *DOWN = Pull DOWN* | *UP = Pull UP* |
|---|---|---|
| SW1 = s_rst | PICMG_RST | DB_RST |
| SW2 = IDSEL | PICMG (top slot) | PCI (top slot) |
| SW3 = pr_4 | PICMG (top slot) | PCI (top slot) |
| SW4 = pr_5 | Enable Prim 64–bit | Disable Prim 64–bit |
| SW5 = pr_6 | ROM Socket | Flash ROM |

## Parallel ROM



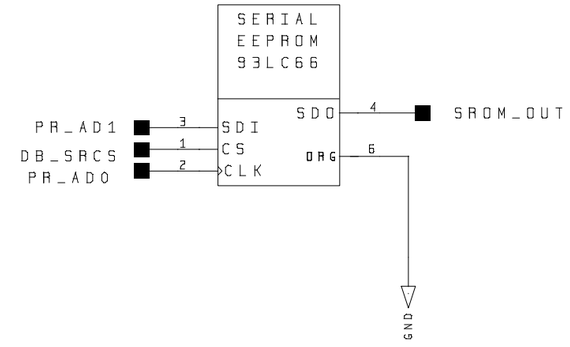

This Socket has a Write Enable Pin So is unsuitable for an EPROM

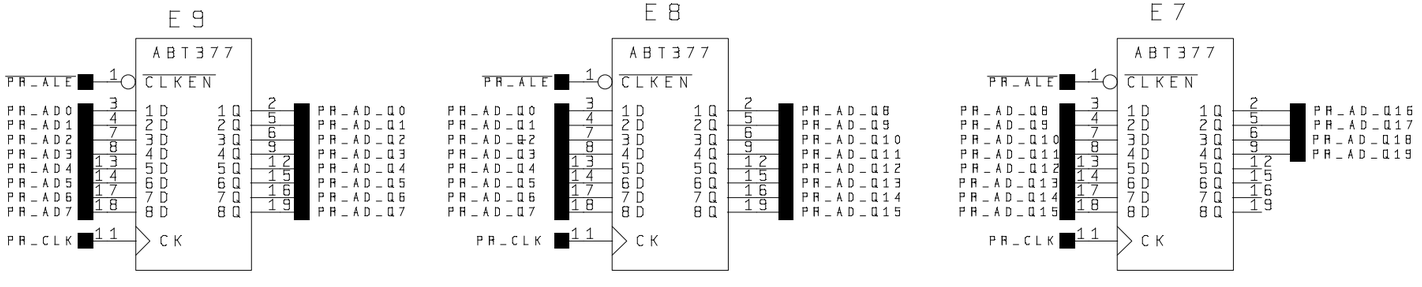



## Serial ROM

E4



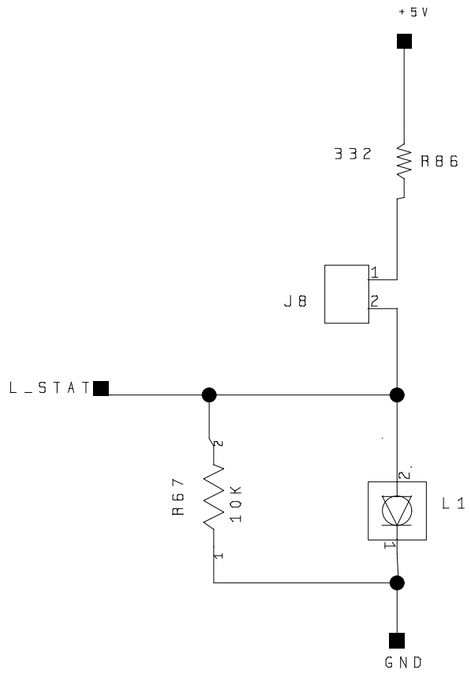



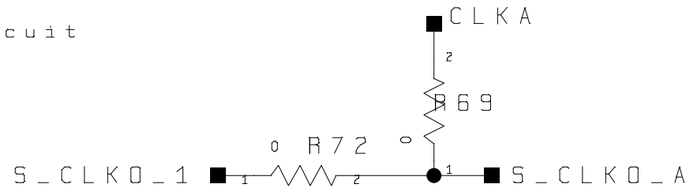

## Parallel ROM Address Latches

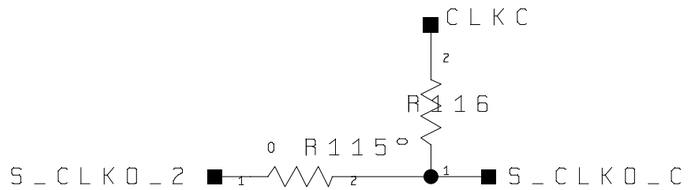
2-24-2000_13:59

| | | | |
|---|---|---|---|
| ENG. SMC | DATE | TITLE: EB555 4 | |
| BOARD LOCATION: | | | |
| SHEET | OF | | |
| TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER | REV. |

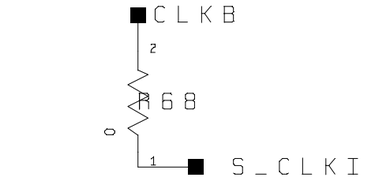
# Compact PCI Hot Swap Test Circuit

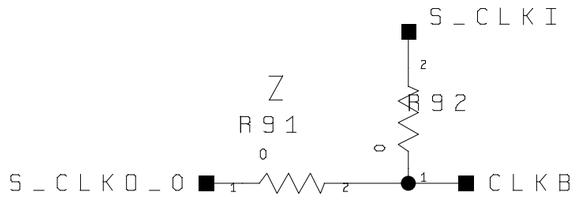



Postional requirement



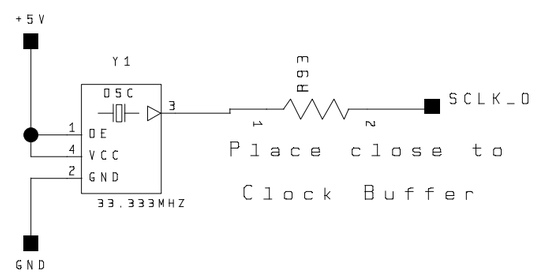



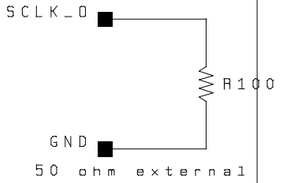

| Central Function | | | |
|---|---|---|---|
| 21554 | | System Slot | |
| In | Out | In | Out |
| R65 | R68 | R68 | R65 |
| R72 | R69 | R69 | R72 |
| R91 | R92 | R92 | R73 |
| R115 | R116 | R116 | R91 |
| | | | R115 |

| External Oscillator | |
|---|---|
| In | Out |
| R93 | R65 |

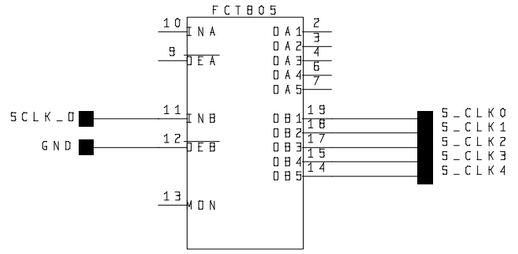
## Clock Generation

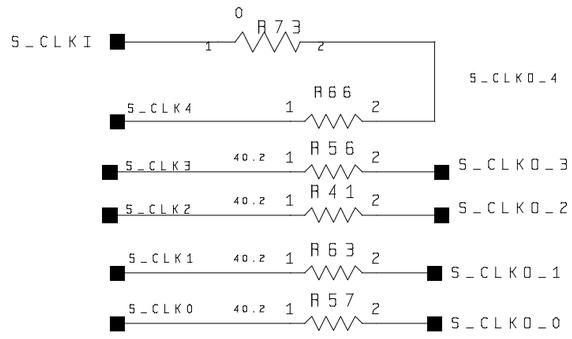
No Connection




E3



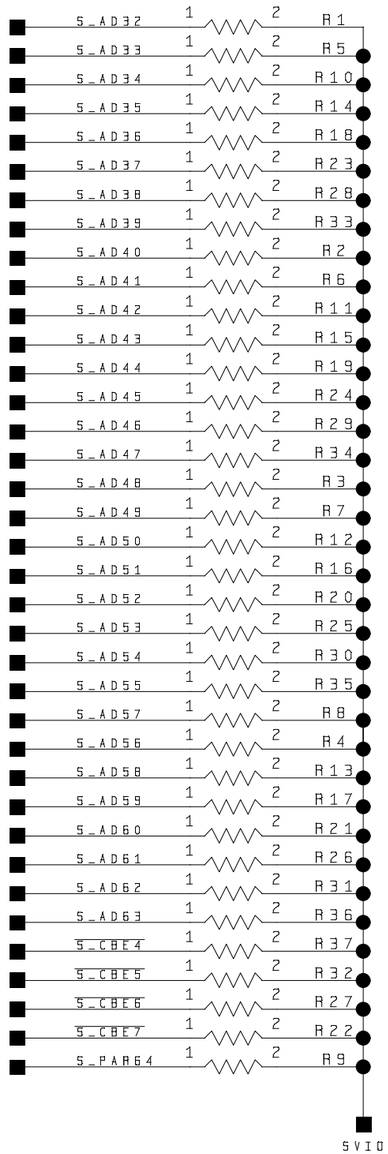




Series resistors should be close to the buffer outputs.
Clock traces should be kept the same length
Keep clock signals on same layer
Avoid vias and other transmission discontinuities

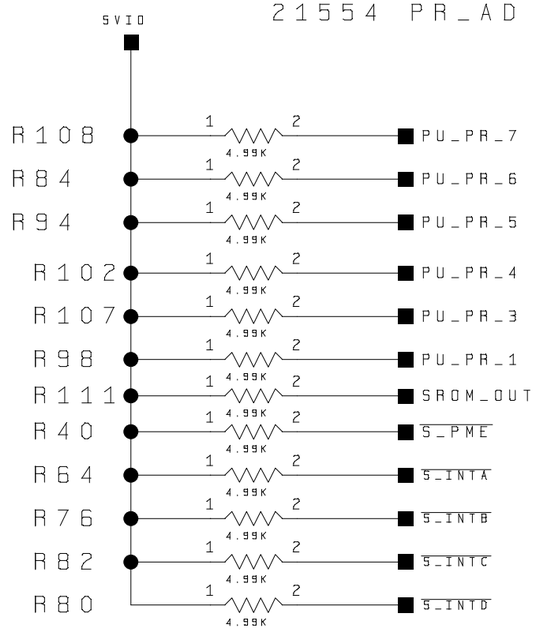
1-19-2000_18:49

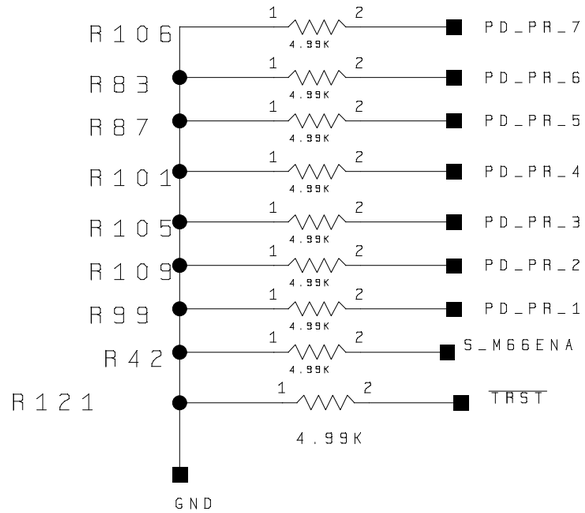
| | | | |
|---|---|---|---|
| ENG. SMC | DATE | TITLE: EB555 5 | |
| BOARD LOCATION: | | | |
| SHEET | OF | | |
| TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER / REV. | |

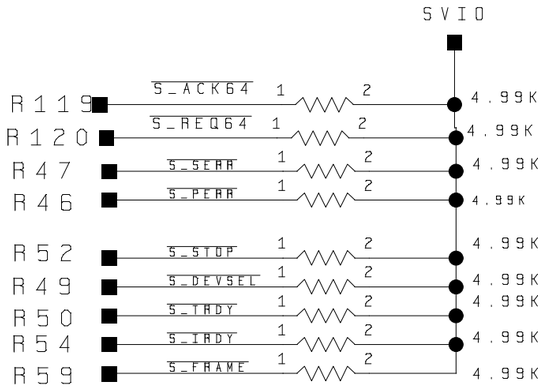
## 64-Bit Pull-Ups
R = 4.99K ohms

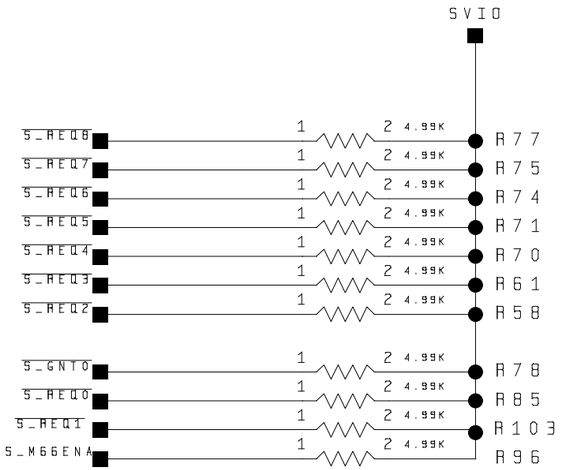



## 21554 PR_AD and Misc Pull-Ups/Downs




2-24-2000_13:59

| | | | |
|---|---|---|---|
| ENG. SMC | DATE | TITLE: EB555 6 | |
| BOARD LOCATION: | | | |
| SHEET OF | | | |
| TOP DOCUMENT NUMBER: | SIZE B | CODE | NUMBER REV. |

21-PCI64-00

Primary PCI Edge Connector

J3

PCI_U_64

NOTE: PRSNT1 Grounded

KEY

KEY

KEY

KEY

KEYWAY

KEYWAY

P_ACK64

P_M66ENA

P_LOCK

P_PME

P_PME Input

Q1

N-CHAN MOSFET

NOTE: R43, R45, and R114 are not populated as they are the responsibility of the motherboard.

R45 4.99K

R88

R43 4.99K

C23 .022UF

C24 0.1UF

C34 .01UF

C36 .01UF

C47 .022UF

C48 .022UF

C52 .022UF

C56 .022UF

C58 .022UF

C68 .022UF

C72 .022UF

svio generation ckt

R97 0

R95 0

SVIO

0.22UF C78 0.22UF C61 0.22UF C10 0.22UF C79

Place 1 0.22uf Cap close to each of the Connectors on Pages 9, 10, & 11

Place this capacitor near pin B19 of connector this page.

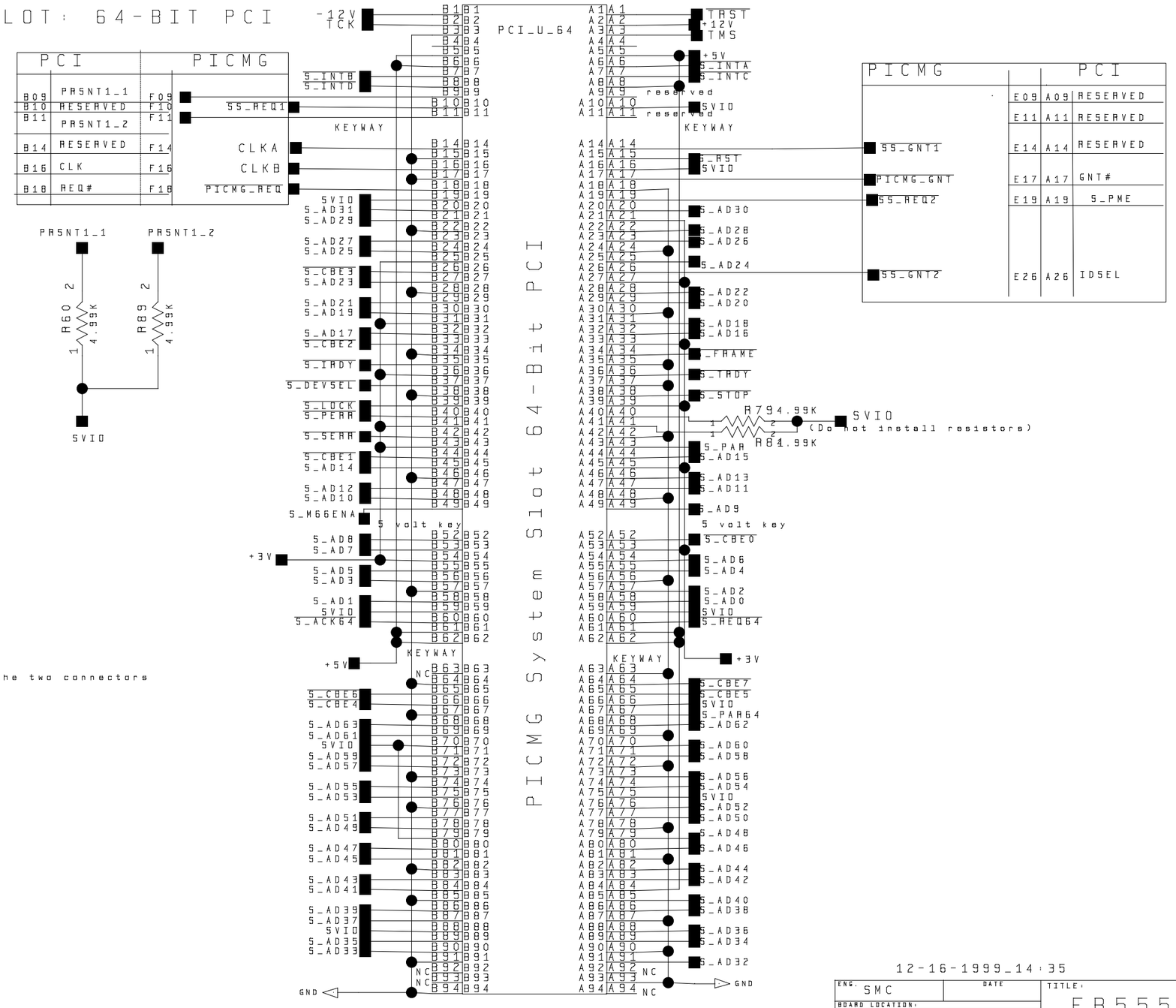
C76 0.22UF

12-16-1999_14:50

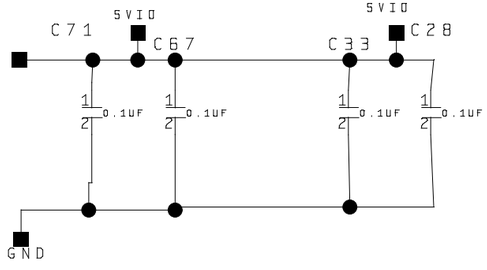
| | | | |
|---|---|---|---|
| ENG. SMC | DATE | TITLE: EB555 | 7 |
| BOARD LOCATION: | | | |
| SHEET | OF | | |
| TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER / REV. | |

# SYSTEM SLOT: 64-BIT PCI

J101
12-39839-19

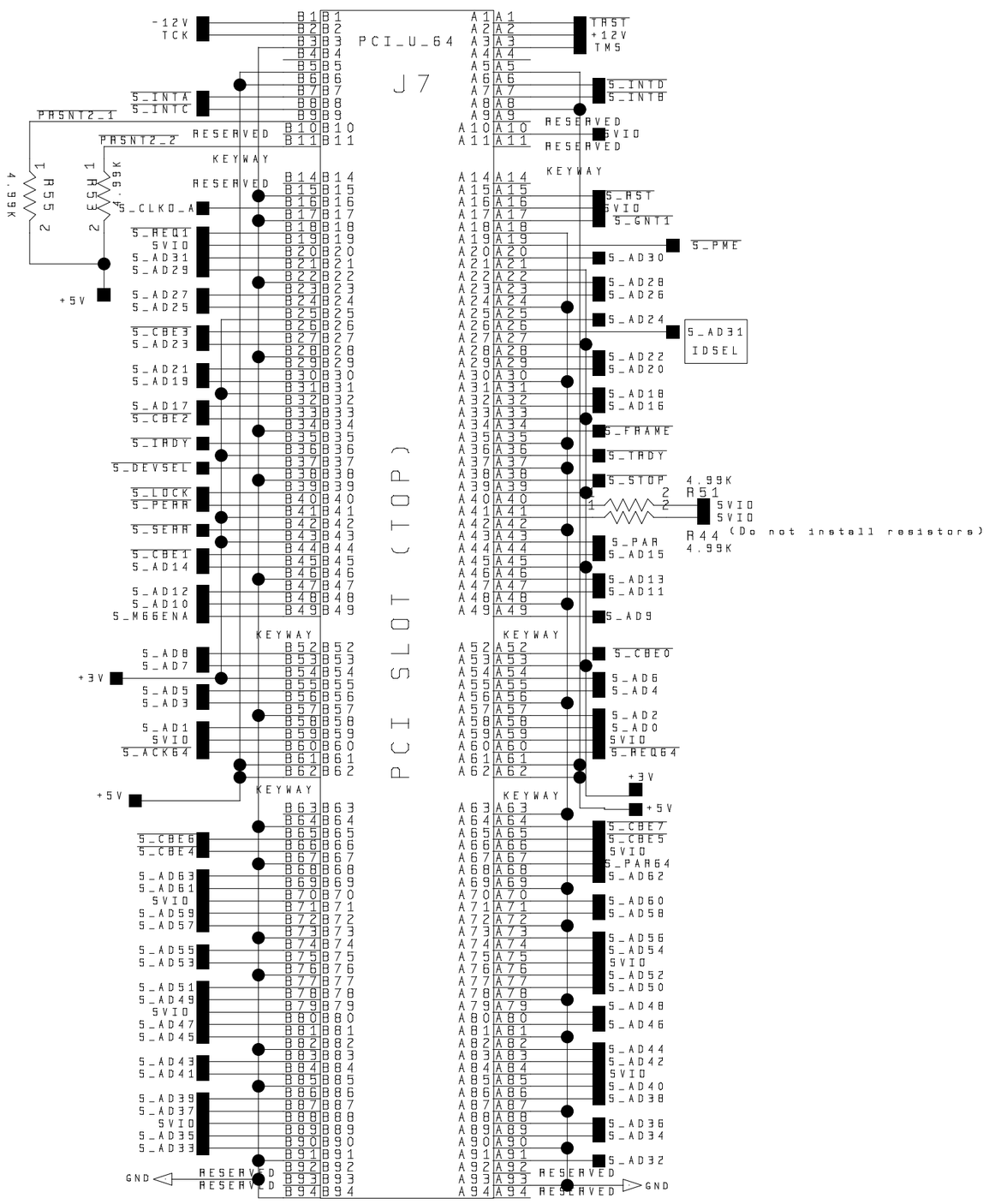


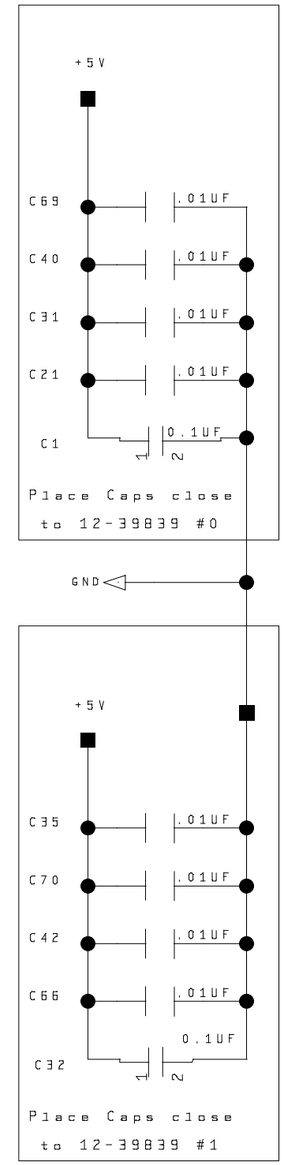

Put two 0.1uF and two 0.22uF close to each of the two connectors




12-16-1999_14:35

| | | | |
|---|---|---|---|
| ENG. SMC | DATE | TITLE: EB555 | 8 |
| BOARD LOCATION: | | | |
| SHEET | OF | | |
| TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER / REV. | |



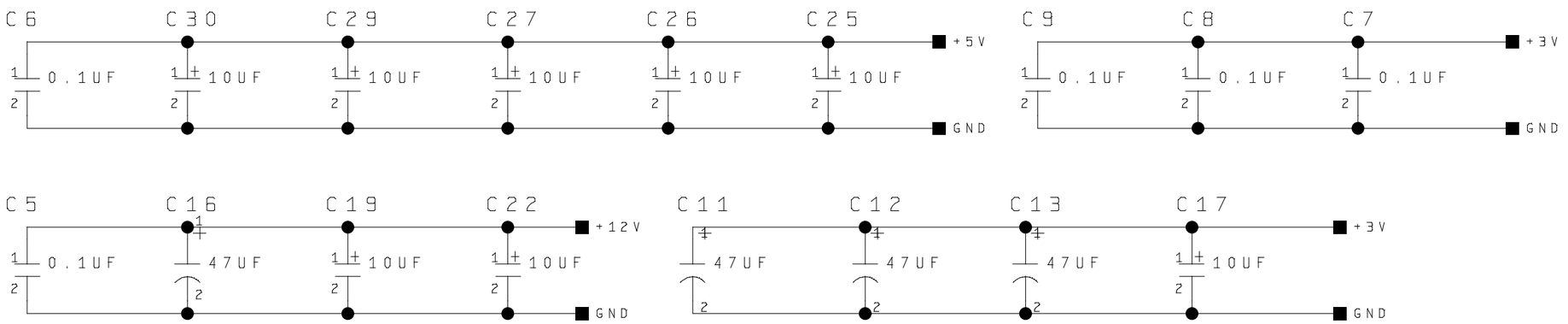




Mount 15uf Cap close to card edge

12-16-1999_14:51

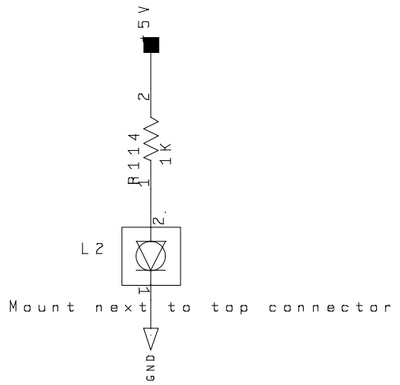
| | | | | | |
|---|---|---|---|---|---|
| ENG. GWRD | DATE | TITLE: EB555 9 | | | |
| BOARD LOCATION: | | | | | |
| SHEET OF | | | | | |
| TOP DOCUMENT NUMBER: | | SIZE B | CODE | NUMBER | REV. |

## Decoupling; bulk, for all power planes



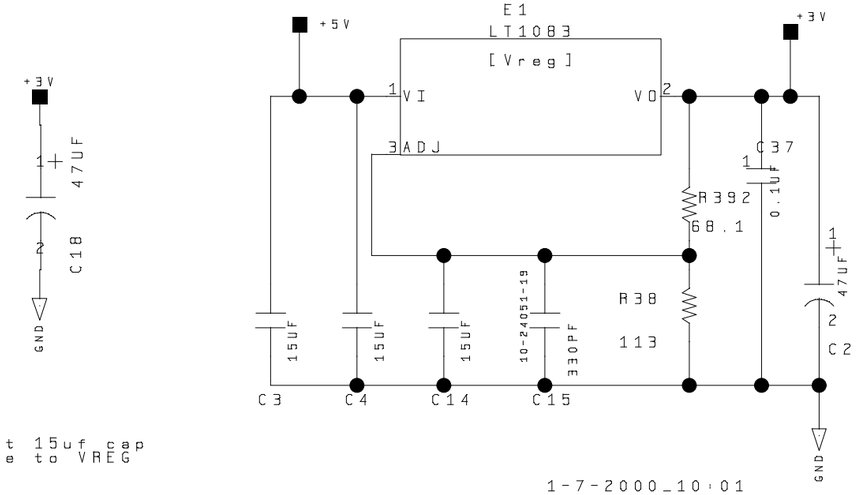


Earth Ground Holes




Mount next to top connector

## Power regulation (3.3V)



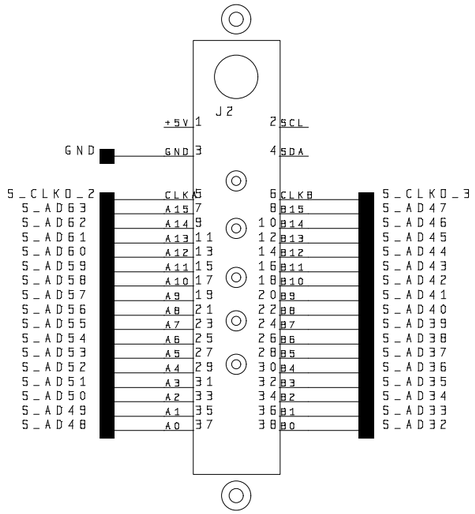

Mount 15uf cap close to VREG

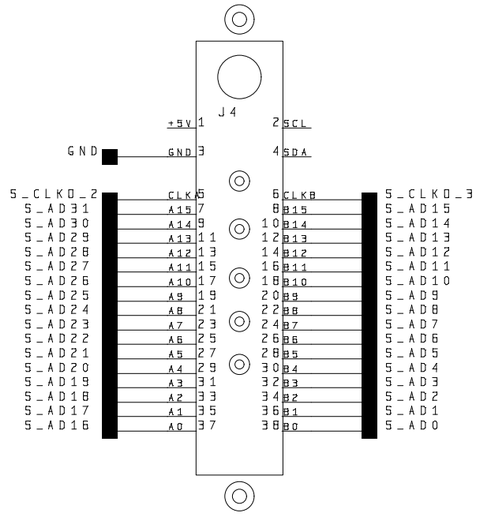
1-7-2000_10:01

1-7-2000_10:01

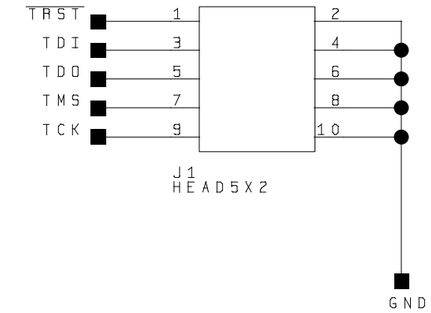
| | | | |
|---|---|---|---|
| ENG. SMC | DATE | TITLE: EB555 | 10 |
| BOARD LOCATION: | | | |
| SHEET | OF | | |
| TOP DOCUMENT NUMBER: | | SIZE B / CODE / NUMBER / REV. | |

## Secondary AD Signals

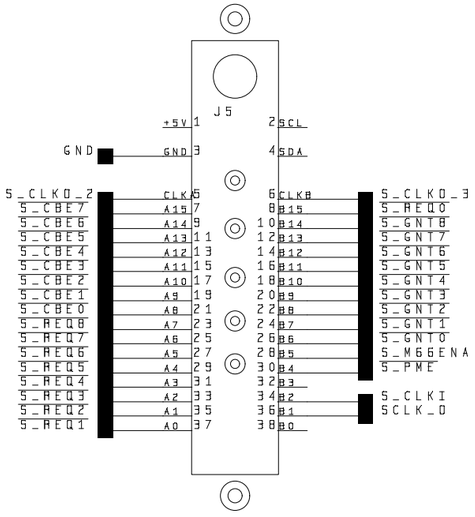


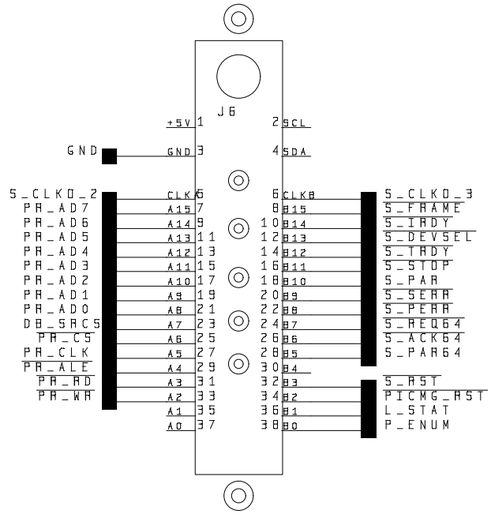

## JTAG Connections




## CBE, REQ, and GNT Lines




## ROM and Control Lines

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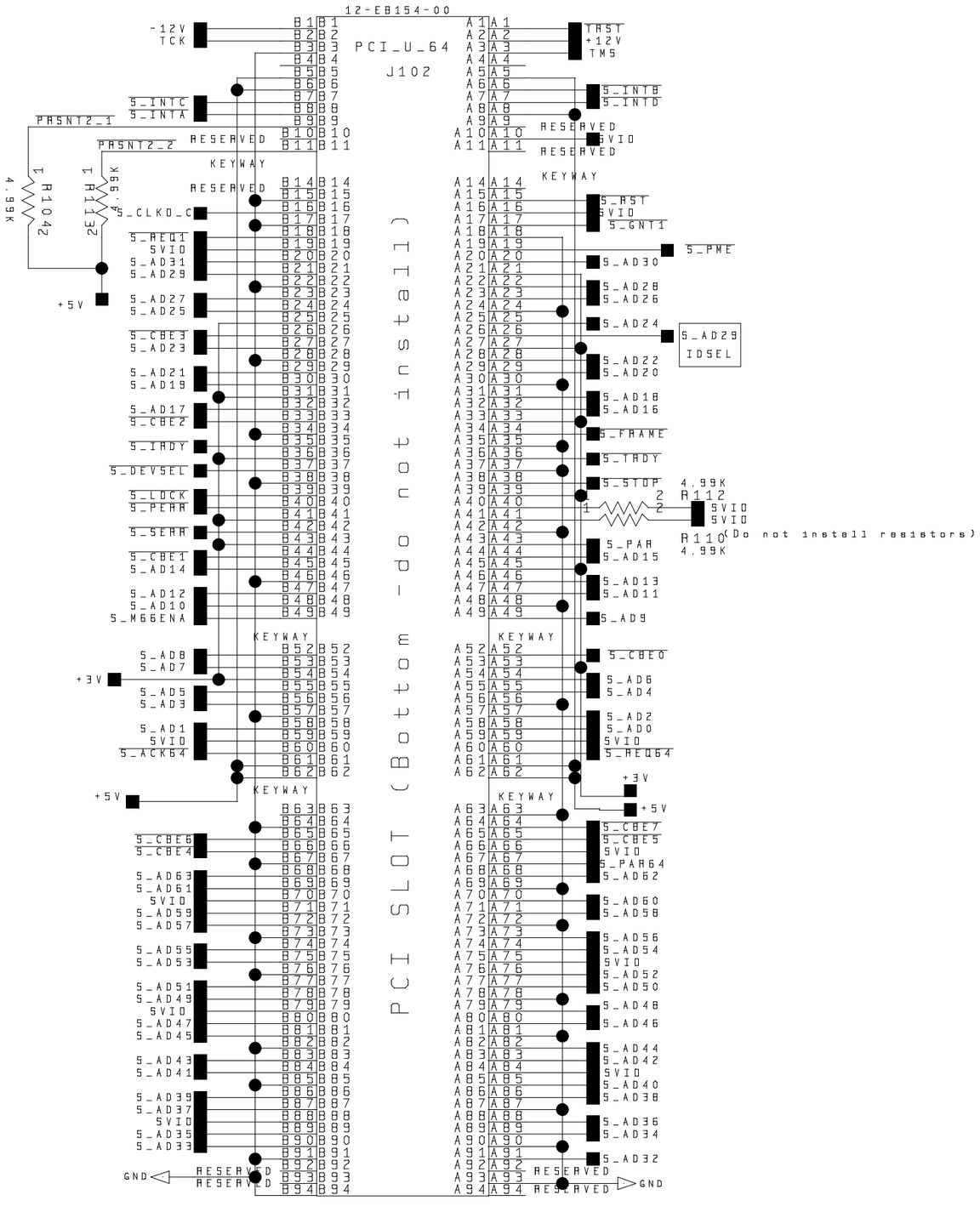


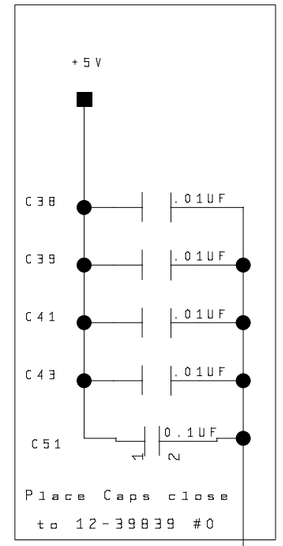


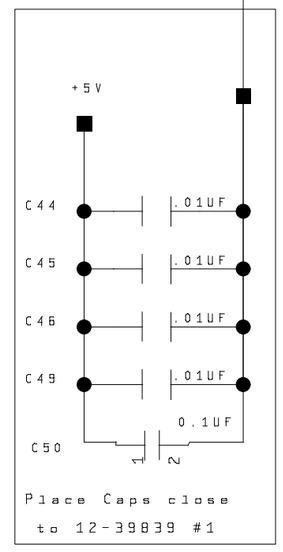


GND

15UF C53

+5V GND

Mount 15uf Cap close to card edge

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| | | | |
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